CPRE 4910 Weekly Report 02

9/19/2025 – 10/06/2025

Group number: SDMay26-24

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

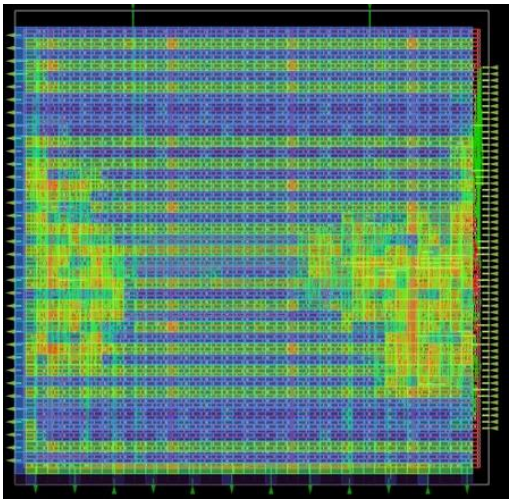
Colin McGann	***-Project Lead***
Samuel Forde	***-PCB & Layout Lead***
Michael Drobot	***-Firmware Lead***
Jack Tonn	***-Testbench and Validation Lead***
Dawud Benedict	***-Toolflow Lead***
Emil Kosic	***-Repository and Coding Standards Lead***
Joshua Arceo	***-Client/Advisor Communications Lead***

- **Weekly Summary**

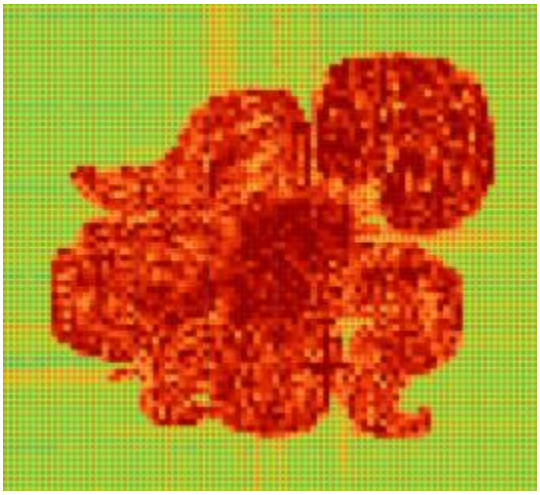
This week, we continued to scope the project and started doing design work on the GPU. The verification team searched through popular HDL verification packages and made a table comparing them. The PCB design team created a high-speed memory and VGA PMOD board. We also wrote the HDL for a SPI memory controller and rasterizer and worked on the Chipforge digital tutorials to further our understanding of how to complete our project.

- **Past week accomplishments**
    - Colin McGann: Wrote the rasterizer and SPI memory controller modules. Got depth buffer and write stripe caching working with the rasterizer. Developed a virtual vga verilog module for debugging video outputs. Did some basic performance analysis on the early rasterizer

      SPI Memory Controller:



Rasterizer:



- Michael Drobot: Redesigned the VGA/Memory PMOD PCB to use 3 memory chips directly connected to the host. Upgraded CICD on the hardware repository to KiCad 9.0. Ordered hardware. Began designing the VGA output module.
- Samuel Forde: Worked on doing a write-up on vertex shading, and the operations necessary, started writing MAC units for vertex shading performance comparison. Final results should be factored into final presentation, or final design doc.

- Jack Tonn:

  Led the research on verification methods to create the table below:

Verification Tool	**Ease of Use**[1]	**Ease of Implementation**[2]	**Notes**	**How recommended is it?**

Waveforms	Very Low	Very High	Good for debugging, bad for formal verification	Very Low
CocoTB	High	High	Caravel already encourages it & has it implemented in the file system	High
UVM	Low	In progress, but so far, no issues. Doesn't seem too bad.	UVM allegedly works well with Questa. Code Coverage	High
SVUnit	High	Mid	"Allegedly" can show coverage	Very High

For this table, I wrote testbench for an adder in different validation tools and compared how easy it was to integrate the design into our toolflow, and how easy it was to actually write the testbench and get the results back.

- Dawud Benedict: Researched UVM implementation into QuestaSim CLI and Toolchain. Got an adder designed in Caravel harness to prepare for a real design.
- Emil Kosic: Continued Chipforge Tutorials, completed Tutorials 1-3.
- Joshua Arceo: Worked on team website, worked through more ChipForge

- **Pending issues**
  - Integrating existing testbenches in SVUnit
  - Optimize the rasterization pipeline and finish texture sampling
- **Individual contributions**

NAME	Individual Contributions	Hours these weeks	HOURS cumulative
Colin McGann	Rasterizer, SPI Controller, Virtual VGA	20	40
Michael Drobot	MemoryVGAPmod redesign, CICD fixes	10	12

Samuel Forde	Write-up/presentation on vertex shaders	8	12
Jack Tonn	Verification table and testbenches	15	20
Dawud Benedict	UVM with Questa CLI, finished adder project	10	14
Emil Kosic	Continuing Chipforge tutorials	7	12
Joshua Arceo	More Chipforge tutorials, worked on team website	8	11

- **Comments and extended discussion**
  - None
- **Plans for the upcoming week**
  - Michael Drobot: Design review for the PMOD board with peers and faculty advisor. Order board and parts.
  - Dawud Benedict: Start designing a Wishbone to PKBus (Wishbone Slave, PKBus Master). Get a simple UVM testbench working with Questa CLI for the toolchain.
  - Josh Arceo: Finish Chipforge tutorials and begin working on the ISA
  - Jack Tonn: Write unit tests for Rasterizer and SPI controller, research code coverage techniques
  - Colin McGann: Keep working on the rasterizer to get optimal performance. Convery my testbenches over to our new test framework
  - Samuel Forde: Finish up vertex shaders presentation, start writing Verilog
  - Complete Chipforge tutorials, conduct research for GPU ISA and create a table of instruction recommendations.

- **Summary of weekly advisor meeting**

The following is a list of questions and comments of particular note said during the meeting.

- Choose a high-level architecture, choose a testing framework, and review hardware designs.
- What will our core ISA look like? What operations do we need to support
- What can our users do with the programmable core ISA? Can we practically do ray tracing?
- How will the cores handle branching? How many layers of branching will be allowed if doing predicate logic?
- What registers will be global and what registers will be local to cores?
- What technology will the caches be made of in the cores

Overall, the meeting was productive and gave us plenty of tasks and considerations to make as we continue to flesh out our design and start to implement it in our repository.